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AMENDMENTS TO THE SPECIFICATION

Please make the following amendments to the paragraph beginning on page 14, line 25 and ending on page 15, line 2:

A1
Figure 8 illustrates a preferred embodiment of a buffer memory controller 830 augmented to perform non-sequential reads from the buffer memory 206 through a single command from the microprocessor 204. The buffer memory controller 830 preferably includes all of the components illustrated in Figure [[4]] 5 of the buffer memory controller 230. The buffer memory controller 830 also preferably includes a set of address registers 852, a working disk formatter buffer address register 802, a set of block count registers 862, a working block count register 864, a busy flag 854, and combined write logic 870.